DELAY LINE AND OUTPUT CLOCK GENERATOR USING SAME

ABSTRACT

[00100] A delay line for an adjustable, high speed clock generator is based on two-stage multiplexing, in which for all pairs of adjacent taps, a change from a current tap to an adjacent tap in the pair is executed by switching only one of the first stage and second stage multiplexers. Control signals are generated for the first and second stage multiplexers by logic based on bidirectional shift registers. The delay line is suitable for generation of an output clock having an adjustable phase, allowing for smooth, glitch-free adjustment over a large range of phases.